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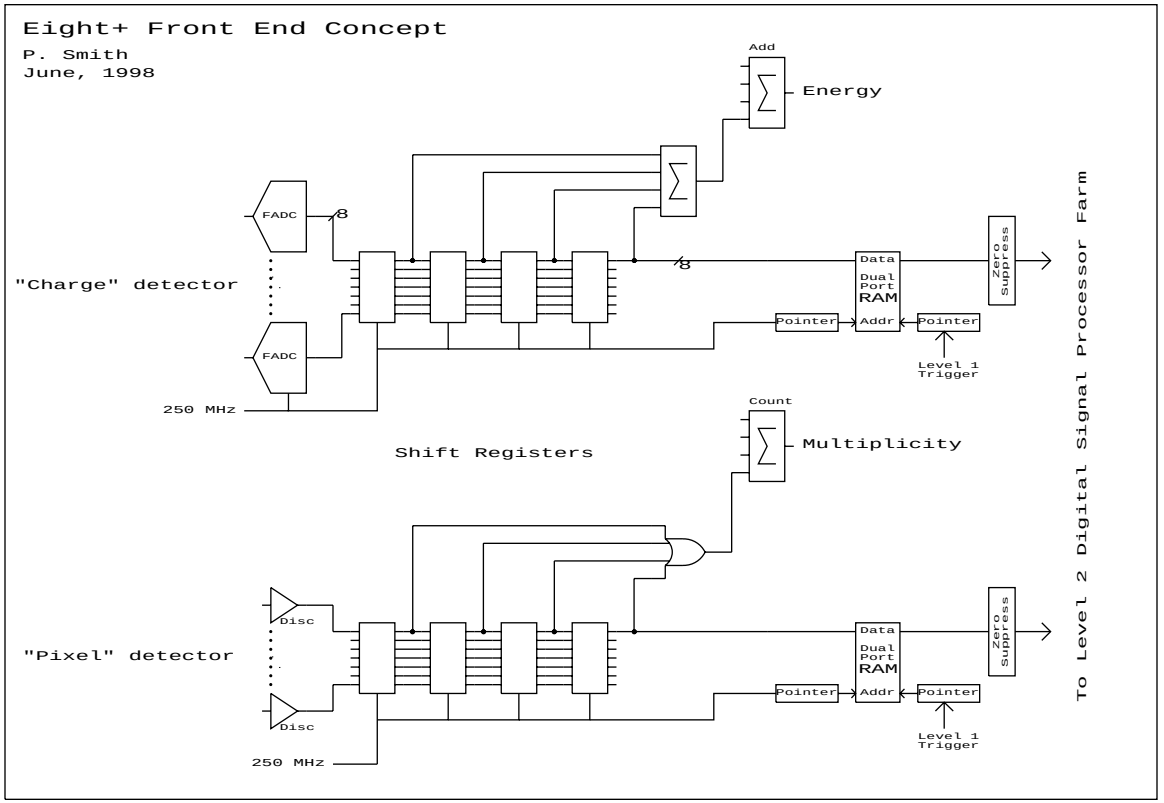
Proposed Hall D Detector Electronics

With nearly 10**5 channels, the signal processing and data acquisition electronics system will present a significant challenge. We envisage much of the electronics being physically located on or near the detectors to avoid the long and expensive low-level signal cables otherwise required. CERN detectors such as COMPASS and ATLAS provide a good model, and we should build on their experience as much as possible. Radiation hardness and minimal power dissipation are additional constraints. The high beam rate will necessitate good time resolution, integrated low level triggering capability and sufficient pipelining of the data to accomomdate the trigger decision time.

A proposed architecture is shown in the figure. Detector channels are either "pixels", e.g. PWCs, drift chambers, and ring cerenkovs, or charge detectors, e.g. CSI or lead glass. Pixel detectors are discriminated, while charge detectors are digitized by Flash ADCs (FADC). The digitized information is pipelined in shift registers which provide a time window for the first level of triggering to consider. After passing through the shift registers, the data are further pipelined in RAM to provide time for the level 1 trigger decision. In the event of a level 1 trigger, the RAM contents are transferred to a level 2 processor farm where more detailed trigger decisions take place.


Eight+ Front End Concept
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Add
Energy
FADC
8
"Charge" detector
FADC
8
Data
Dual
Port
RAM
Addr
Pointer
Pointer
Zero
Suppress
Level 1
Trigger
250 MHz
Count
Multiplicity
Shift Registers
Disc
"Pixel" detector
Disc
Data
Dual
Port
RAM
Addr
Pointer
Pointer
Zero
Suppress
Level 1
Trigger
250 MHz
To Level 2 Digital Signal Processor Farm